

FIG. 1

FIG.2A

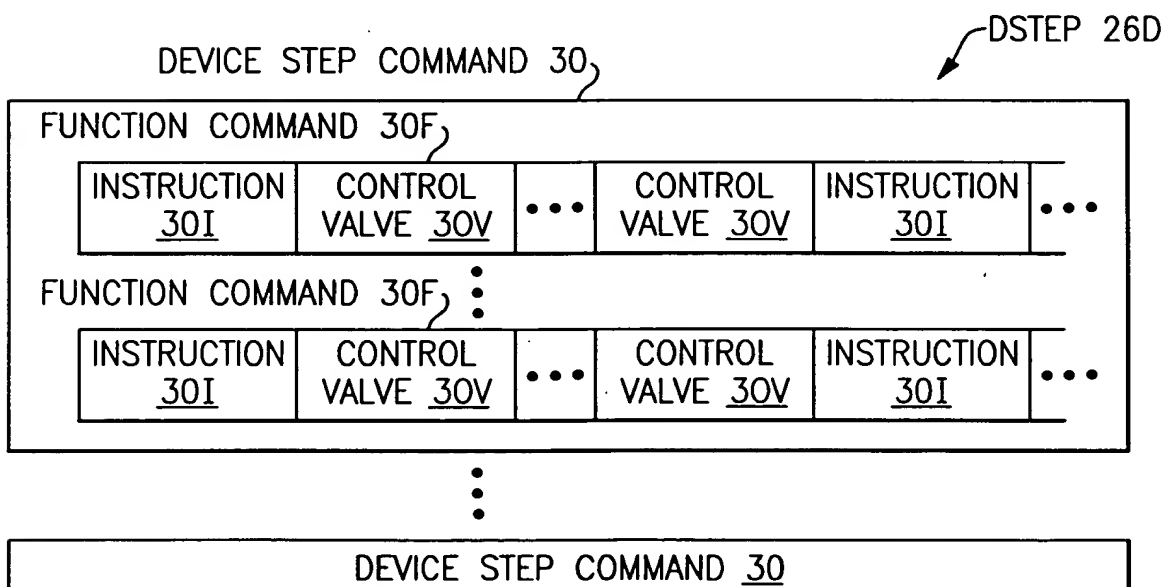
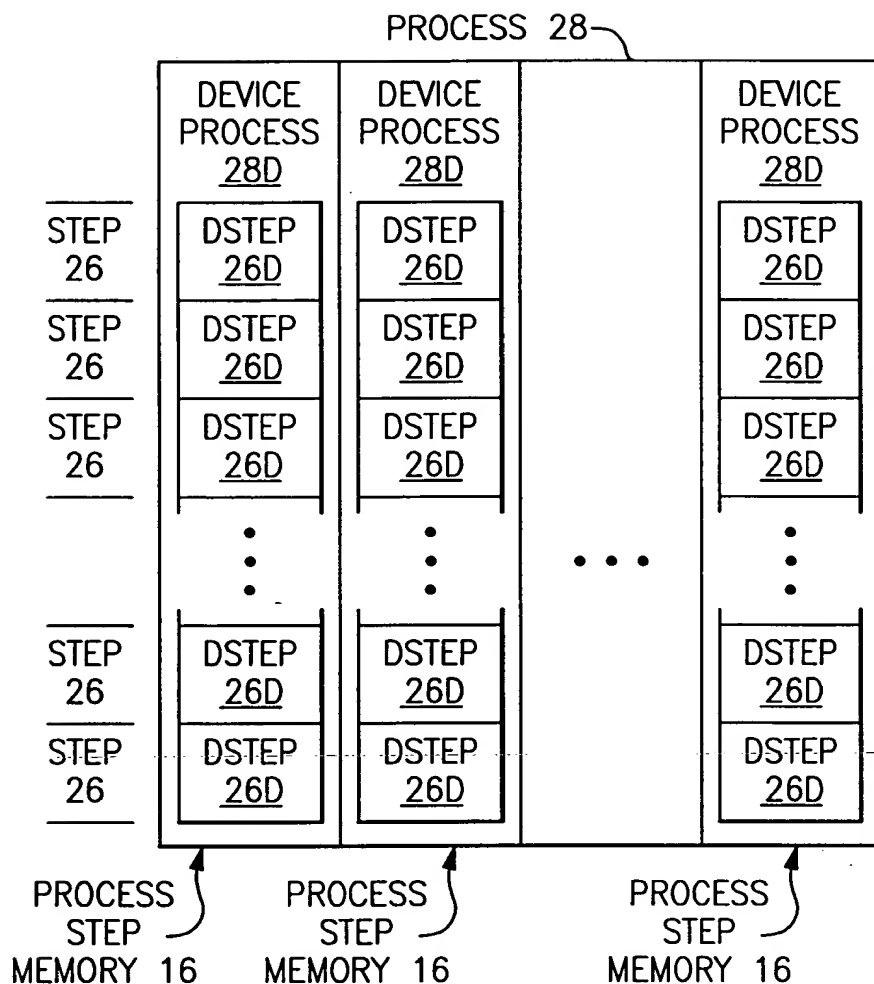


FIG.2B

FIG. 3

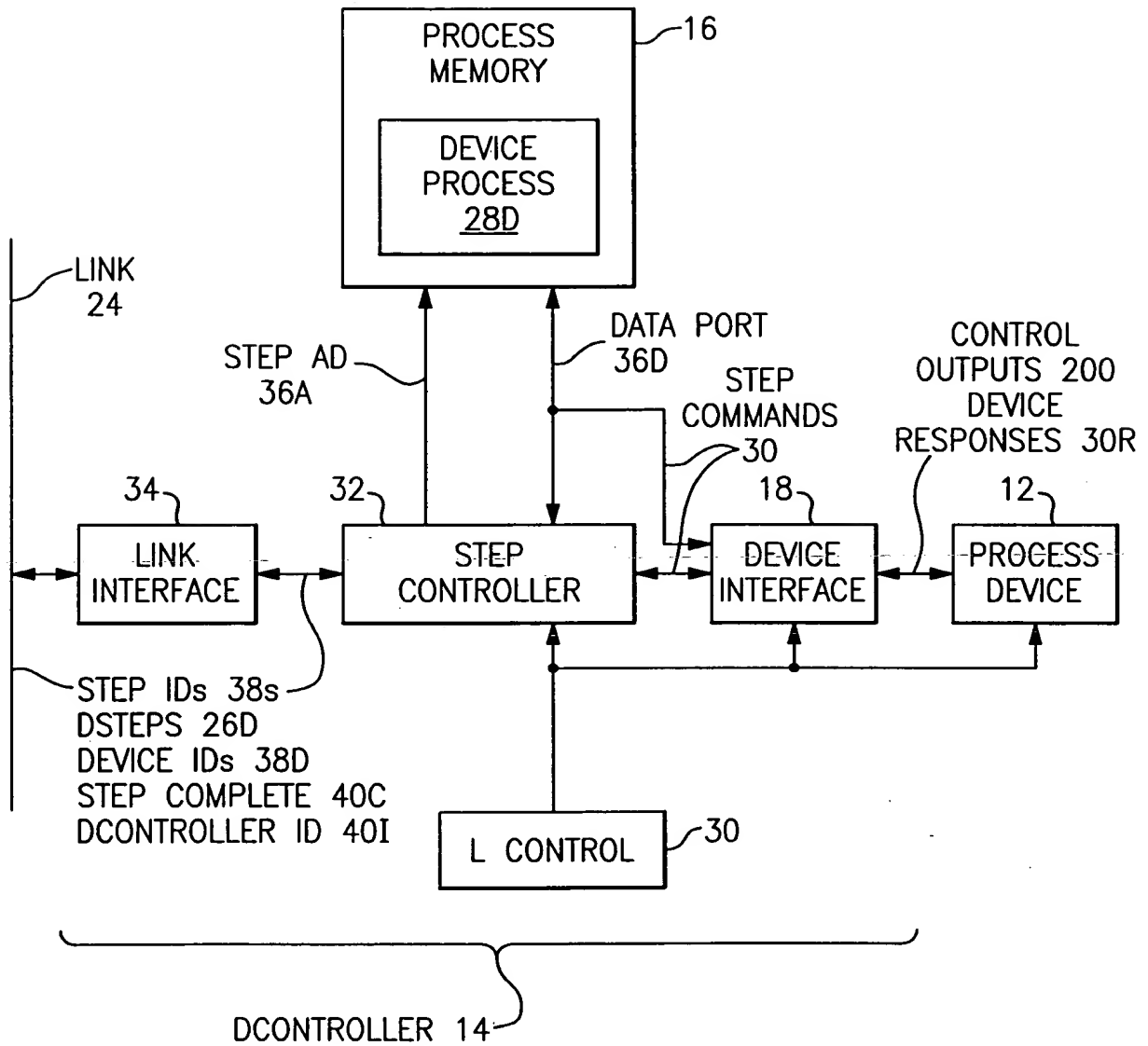


FIG.3

```
graph TD
    MM[MASTER MEMORY 46] <--> CP[COMMAND PROCESSOR 42]
    subgraph CP [COMMAND PROCESSOR 42]
        SG[STEP GENERATOR 48]
    end
    CP <--> LI[LINK INTERFACE 34]
    LI <--> L[LINK 24]
    LI -- "STEP IDs 38s, DPROCESSES 28D" --> CP
    subgraph Bus
        ID1[INPUT DEVICE 44]
        ID2[INPUT DEVICE 44]
        ID3[INPUT DEVICE 44]
    end
    Bus <--> CP
```

FIG.4

FIG.5